## FEATURES

95\% peak efficiency
Optimized for low output voltages
Optimized for extremely small ceramic inductors
Up to 600 mA , load current
2.7 V to 5.5 V input voltage range

Operates with a Single Li-Ion battery
Fixed Output Voltage from 0.8 V to 1.875 V
Adjustable Output Voltage from 0.8 V to 1.875 V
Low $60 \mu \mathrm{~A}$ quiescent current
Internal Synchronous rectifier
3 MHz Operating Frequency
$0.1 \mu \mathrm{~A}$ Shutdown Supply Current
Small 8-Lead $3 \times 3$ LFCSP Package
Enable /shutdown logic input
Under Voltage Lockout
Internal Soft Start
Internal Compensation

## APPLICATIONS

Wireless Handsets
Portable Media Players
PDA's and Palmtop Computers
Digital Cameras
Smart Phones

TYPICAL PERFORMANCE CHARACTERITICS


Figure 1.

## GENERAL DESCRIPTION

The ADP2102 is a low quiescent current step-down DC-DC converter optimized to regulate low output voltages in a compact 3mmx3mm LFCSP package. At high load currents, the ADP2102 uses a current mode, constant on time, pseudo fixed frequency, valley current control scheme for excellent stability and transient response with very few, small external components. To ensure the longest battery life in portable applications, the ADP2102 has a power saving mode that reduces the switching frequency under light load conditions to significantly reduce the quiescent current.
The ADP2102 runs from input voltages from 2.7V to 5.5 V allowing single $\mathrm{Li}+/ \mathrm{Li}-$ polymer cell, multiple Alkaline/Ni-MH cells and other standard power sources. ADP2102 output voltage is adjustable from 0.8 V to 1.875 V , while the suffix part numbers ADP2102-XX indicate pre-set voltage ranges of 1.875 , $1.8,1.5,1.375,1.25,1.2,1.0 \& 0.8 \mathrm{~V}$. All versions include an internal power switch and a synchronous rectifier for high efficiency while internal compensation guarantees minimal number of external components. During logic-controlled shutdown, the input is disconnected from the output and it draws less than $0.1 \mu \mathrm{~A}$ from the input source. Other key features include under voltage lockout to prevent deep battery discharge and soft start to prevent input current overshoot at startup.

TYPICAL APPLICATION CIRCUIT


Figure 2.

## Preliminary Technical Data

## SPECIFICATIONS

$\mathrm{V}_{\mathrm{IN}}=3.6 \mathrm{~V}$, Bold values indicate $\mathrm{T}_{\mathrm{J}}=-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$, unless otherwise noted. ${ }^{1}$
Table 1.

| Parameters | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Input Voltage Range ${ }^{2}$ |  | 2.7 |  | 5.5 | V |
| Under voltage Lockout Threshold | VIN rising | 2.2 | 2.4 | 2.5 | V |
| Under voltage Lockout Hysterisis |  |  | 200 |  | mV |
| Output Voltage Range | ADP2102_Fixed | 0.8 |  | 1.875 | V |
| Output Voltage Accuracy |  | -1 |  | 1 | \% |
| Load Regulation | Vout $=0.8 \mathrm{~V}-1.875 \mathrm{~V}$, , load $=0-600 \mathrm{~mA}$ |  | 0.3 | 0.5 | \% |
| Line Regulation | lout $=10 \mathrm{~mA}$ |  | 0.3 | 0.6 | \% |
| FB Regulation Voltage |  | 784 | 800 | 816 | mV |
| FB Bias current |  |  | 1 | 50 | nA |
| Operating Current | ADP2102, $\mathrm{V}_{\mathrm{FB}}=0.9 \mathrm{~V}$ |  | 60 | 80 | $\mu \mathrm{A}$ |
| Shutdown Current | $\mathrm{EN}=0 \mathrm{~V}$ |  | 0.1 | 1 | $\mu \mathrm{A}$ |
| Output Current |  |  |  | 600 | mA |
| LX On Resistance | P-Channel Switch |  | 300 | 600 | $m \Omega$ |
|  | N-channel Synchronous Rectifier |  | 250 | 400 | $\mathrm{m} \Omega$ |
| LX Leakage Current | $\mathrm{PV} \mathrm{V}_{\text {IN }}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{Lx}}=0 \mathrm{~V}, 5.5 \mathrm{~V}$ |  |  | 1 | $\mu \mathrm{A}$ |
| LX Minimum -Off Time |  |  | 100 |  | ns |
| Forward Current Limit | P-Channel Switch or N-Channel Synchronous Rectifier |  |  |  |  |
| EN,MODE Input High Threshold |  | 1.3 |  |  | V |
| EN,MODE Input Low Threshold |  |  |  | 0.4 | V |
| EN,MODE Input Leakage Current | $\mathrm{EN}=\mathrm{MODE}=0,5.5 \mathrm{~V}$ | -1 | 0.1 | 1 | $\mu \mathrm{A}$ |
| Switching Frequency |  |  | 3 |  | MHz |
| Soft Start Period |  | 250 | 500 | 800 |  |
| Thermal Shutdown Threshold |  |  | 150 |  | ${ }^{\circ} \mathrm{C}$ |
| Thermal Shutdown Hysterisis |  |  | 15 |  | ${ }^{\circ} \mathrm{C}$ |

[^0]
## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
| :--- | :--- |
| AVIN,EN,MODE,FB/OUT to AGND | -0.3 V to +6 V |
| LX to PGND | -0.3 V to $+(\mathrm{V}$ IN $+0.3 \mathrm{~V})$ |
| PVIN to PGND | -0.3 V to +6 V |
| PGND to AGND | -0.3 V to 0.3 V |
| AVIN to PVIN | -0.3 V to 0.3 V |
| Operating Ambient Temperature Range | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}^{1}$ |
| Operating Junction Temperature | $125^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Soldering Conditions | JEDEC J-STD- 020 |

${ }^{1}$ In applications where high power dissipation and poor thermal resistance are present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ( $\left.\mathrm{T}_{\mathrm{A}(\mathrm{MAX})}\right)$ is dependent on the maximum operating junction temperature $\left(\mathrm{T}_{\text {(MAXOP) })}\right)=125^{\circ} \mathrm{C}$ ), the maximum power dissipation of the device ( $\left.\mathrm{P}_{\mathrm{D}(\text { MAX })}\right)$, and the junction-to-ambient thermal resistance of the part/package in the application $\left(\theta_{\mathrm{JA}}\right)$, using the following equation: $\mathrm{T}_{\mathrm{A}(\text { MAX })}=\mathrm{T}_{\text {(MAXOP) })}-\left(\theta_{\mathrm{JA}} \times \mathrm{P}_{\mathrm{D}(\text { MAX })}\right)$.
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages referenced to GND.

## THERMAL RESISTANCE

Table 3. Thermal Resistance

| Package Type | $\boldsymbol{\theta}_{\mathrm{JA}}{ }^{1}$ | Unit |
| :--- | :--- | :--- |
| 8-Lead LFCSP | 54 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |
| Maximum Power Dissipation | 1 | W |

${ }^{1}$ Junction-to-ambient thermal resistance $\left(\theta_{\mathrm{JA}}\right)$ of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is application and board-layout dependent. In
applications where high maximum power dissipation exists, attention to thermal board design is required. The value of $\theta_{\mathrm{JA}}$ can vary depending on PCB material, layout, and environmental conditions. For more information, please refer to Application Note AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP).

## BOUNDARY CONDITION

Natural convection, 4-layer board, exposed pad soldered to the PCB.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## Preliminary Technical Data

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 3.Pin Configuration
Table 4. Pin Function Descriptions

| Pin <br> No. | Mnemonic | Description |
| :--- | :--- | :--- |
| 1 | MODE | Mode Input. To set the ADP2102 to Forced Continuous Conduction Mode (CCM), drive MODE high. To set the <br> ADP2102 to Power Saving Mode (PSM), drive MODE low. <br> Enable Input. Drive EN high to turn on the ADP2102. Drive EN low to turn it off and reduce the input current to $0.1 \mu A$. <br> This pin cannot be left floating. |
| 3 | ENOutput Sense Input or Feedback Input. For fixed output versions, OUT is the top of the internal resistive voltage <br> divider. Connect OUT to the Output Voltage. For adjustable (non-suffix) versions, FB is the input to the error amplifier. <br> Drive FB through a resistive voltage divider to set the output voltage. The FB regulation threshold is 0.8 V. |  |
| 4 | AGND | Analog Ground. Connect AGND to PGND at a single point as close as to the ADP2102 as possible. <br> 5 |
| 6 | PGND | Power Ground. <br> Switch Output. LX is the drain of the p-channel MOSFET switch and n-channel Synchronous rectifier. Connect the <br> output LC filter between LX and output voltage. <br> Power Source Input. Drive PVIN with a 2.7V to 5.5V power source. <br> 8 |
| PVIN | AVIN | Power Source Input. AVIN is the supply for the ADP2102 internal circuitry. For noise reduction, place an external RC <br> filter between PVIN and AVIN. |

## THEORY OF OPERATION

The ADP2102 is a high frequency synchronous step down dcdc buck converter optimized for battery powered portable applications. It is based on a constant-ON time current mode control architecture with voltage feed forward to null frequency variation with line voltage thus creating a pseudo fixed frequency.
This type of control allows generation of very low output voltages at higher switching frequency and offers a very fast load and line transient response with minimal external component count and size. The ADP2102 provides features like Under Voltage Lock Out, Thermal Shutdown and Short Circuit Protection.

The ADP2102 uses valley current mode control, which helps to prevent minimum-ON time limitations at very low output voltages. This allows high frequency operation resulting in low filter inductor and capacitor values.

## CONTROL SCHEME

The ADP2102's High Side Power Switch ON-time is determined by a one shot timer whose pulse width is directly proportional to output voltage and inversely proportional to the input or line voltage. Another one-shot timer sets a minimum OFF time to allow for inductor valley current sensing,
The constant ON-time one-shot timer is triggered at the rising edge of EN and subsequently when the Low Side Power Switch current is below the valley current limit threshold and the minimum OFF-time one-shot timer has timed out.

While the constant ON-time is asserted, the high side power switch is turned on. This causes the inductor current to ramp positively. After the constant ON-time has completed the high side power switch turns off and the low side power switch turns on. This causes the inductor current to ramp negatively until the sensed current flowing in this switch has reached valley current limit. At this point, the low side power switch turns off and a new cycle begins again with the high side switch turning on provided the minimum OFF-time one shot has timed out.

## CONSTANT ON-TIME TIMER

The constant ON-time timer sets the High Side Switch on time. This fast, low jitter, adjustable one shot varies the ON-time in response to input voltage for a given output voltage. The High Side Switch ON -time is inversely proportional to the input voltage and directly proportional to the output voltage.

Ton $=$ K. (Vout $/$ Vin $) \& F s w=1 / K$
Where " $K$ " is an internally set On-time scale factor constant resulting in a constant switching frequency. As can be seen in the above equation, the steady state switching frequency is
theoretically independent of both the input and output voltages to a first order. Therefore, with line voltage feed forward the constant ON - time control scheme is pseudo fixed frequency. This means the loop switches at a constant frequency until a
load step occurs. When a load step occurs, the constant ONtime control loop responds by modulating the OFF time up or down to quickly get back to regulation. This momentary frequency variation results in a faster load transient response than a fixed frequency current mode control loop of similar bandwidth with similar external filter inductor and capacitor. This is an advantage of constant-ON time control scheme.

As described above the frequency of the constant ON-time control loop remains constant to a first order with line and output voltage. There are some second order effects that cause this frequency to increase slightly with load current.

Resistive voltage losses in the High and Low Side Power Switches, package parasitics, inductor DCR and board parasitic resistance cause the loop to compensate by reducing the OFFtime and there fore increasing the switching frequency with increasing load current.

A minimum OFF-time constraint is introduced to allow the inductor valley current sensing on the synchronous switch.

## FORCED CONTINUOUS CONDUCTION MODE

When the MODE pin is HIGH, the ADP2102 operates in Forced Continuous Conduction Mode. In this mode, irrespective of the load current, the inductor current stays continuous and is the preferred mode of operation for low noise applications. During this mode, the switching frequency stays close to 3 MHz typically. In this mode, the efficiency is lower compared to the Power Save Mode during light loads but the output voltage ripple is minimized.

## POWER SAVE MODE

When the MODE pin is LOW, the ADP2102 operates in Power Save Mode. In this mode, at light load currents, the part automatically goes into reduced frequency operation where some pulses are skipped to increase efficiency while still remaining in regulation. At light loads, a zero crossing comparator truncates the low side switch ON-time when the inductor current becomes negative. In this condition, the part works in Discontinuous Conduction Mode (DCM). The threshold between CCM and DCM is approximately

Iload $($ skip $)=($ Vin- Vout $) /(2 \times L) \times$ Ton
For higher load currents, the inductor current does not cross zero threshold and the device switches to the Continuous Conduction Mode and the frequency is fixed to the nominal value. As a result of this auto -mode control technique, the losses are minimized at light loads, improving the system efficiency.

## CURRENT LIMIT

The ADP2102 has protection circuitry to limit the amount of current flowing through the High Side and the Low Side switches. When the current flowing in the forward direction becomes excessive due to a short on the OUT node to ground
or otherwise, the ADP2102 operates in frequency fold back by increasing the OFF time enough to keep the output current fixed. Therefore, during this fault condition the ADP2102 acts as a constant current source at the current limit of 1A typical.

## SOFT START

The ADP2102 has in internal soft start function that ramps the output voltage in a controlled manner upon startup by limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

## ENABLE

The device starts operation with soft start when the EN pin is brought high. Pulling the EN pin low forces the device into shutdown, with a typical shutdown current of $0.1 \mu \mathrm{a}$. In this mode both the High Side and Low Side Power Switches are turned off, the internal resistor feedback divider is disconnected
and the entire control circuitry is switched off. For proper operation, the EN pin must be terminated and must not be left floating.

## UNDER VOLTAGE LOCK OUT

The under voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the main switch and the synchronous switch under undefined conditions and therefore preventing deep discharge of the battery supply

## THERMAL SHUTDOWN

When the Junction Temperature, Tj , exceeds typically $150^{\circ} \mathrm{C}$, the device goes into Thermal Shutdown. In this mode, the High Side and Low Side Power Switches are turned off. The device continues its operation when the junction temperature when the junction temperature falls below typically $135^{\circ} \mathrm{C}$ again.

## Preliminary Technical Data

## OUTLINE DIMENSIONS

8-Lead Frame Chip Scale Package [LFCSP]<br>$3 \times 3 \mathrm{~mm}$ Body<br>(CP-8)<br>Dimensions shown in millimeters



Figure 4. 8 -Lead Lead Frame Chip Scale Package [LFCSP]
3 mm x 3 mm Body, Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
| :--- | :--- | :--- | :--- | :--- |
| ADP2102 | $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$ | 8-Lead Lead Frame Chip Scale Package [LFCSP] <br> ADP2102-EVAL | Evaluation Board |  |


[^0]:    ${ }^{1}$ All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC). Typical values are at $\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathbb{N}}=3.6 \mathrm{~V}$.
    ${ }^{2}$ This is the $\mathrm{V}_{\text {IN }}$ input voltage range over which the rest of the specifications are valid. The part operates as expected until $\mathrm{V}_{\text {IN }}$ goes below the UVLO threshold.

